Processing and Device Technology
Solutions to the Self-Study Problems

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Lösningarna är av varierande kvalité, har gjort dem under kursens gång så ta det för vad det är och inte som en absolut sanning :)

Lecture 2

7. Describe the main steps to how silicon with EGS quality is obtained

EGS - Electronic Grade Silicon
There are three steps towards getting EGS, poly-cristalline silicon. First you want to remove the oxygen from SiO_2

$$SiO_2(s) + 2C(s) \rightarrow 2CO(g) + Si(s)$$

Now we have pure amorphus silicon. Now we will use a middle step to gain an pure batch of poly-cristalline silicon by removing all of the impurities

$$Si(s) + 3HCl \rightarrow H_2(g) + SiHCl_3(g)$$

$SiHCl_3$ have an low boilingpoint (32°C) which allows us to remove the impurities through fractal distillation

$$SiHCl_3(g) + H_2(g) \rightarrow 3HCl(g) + Si(s)$$

Now we got poly-cristalline silicon

8. Describe the Czrochalski technique.

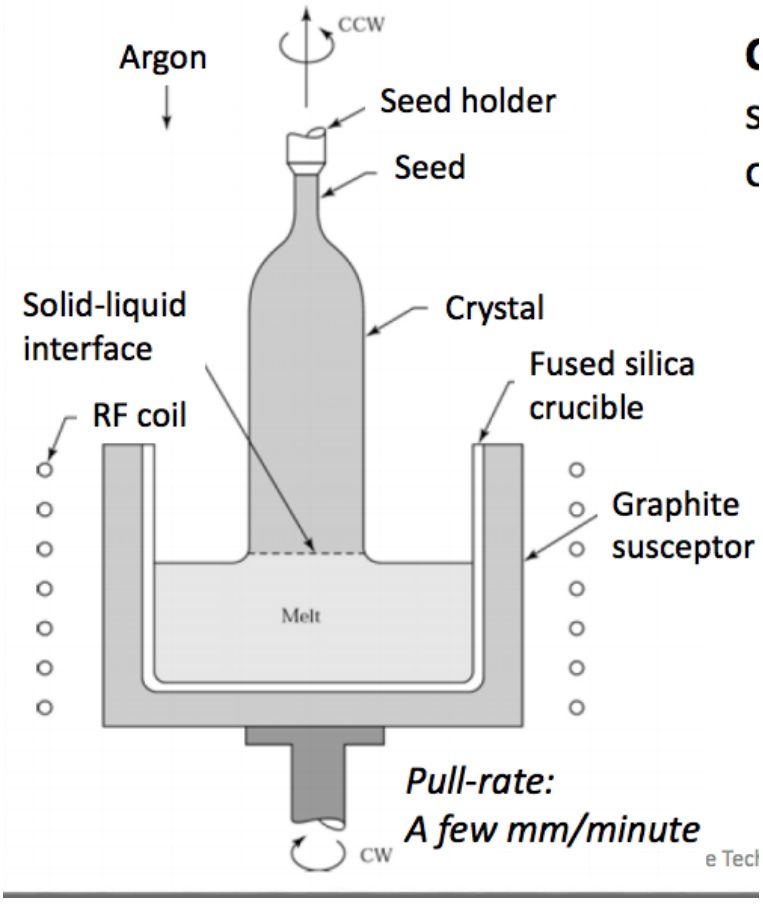


Figure 1:

The seed is dipped in the melt and spun very slowly while the single-crystalline accumulates.

9. Which techniques can be used to grow (bulk) GaAs? – Describe these in a few words

Czochralski technique - same as before although with overpressure of As to prevent As from evaporating

Bridgeman technique - We have a small seed at the cold end that is gradually solidified on by moving the test tube away from the heat. Picture:

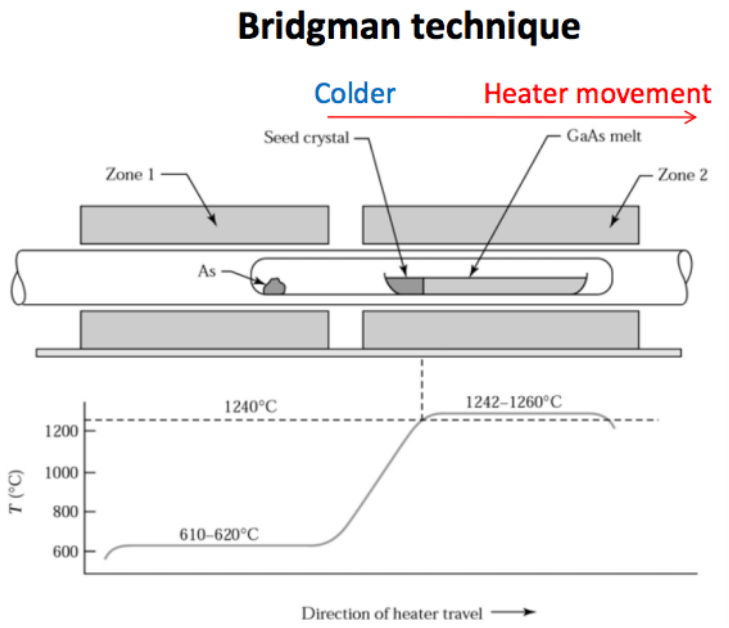


Figure 2:

10. What is the purpose of doping?

To allow electrons/holes to jump the bandgap, to form a current.

11. On a microscopic level, what happens when an impurity, such as arsenic, replaces a silicon atom in a silicon lattice?

You get a hole or a spare electron that can create a current

12. Consider a GaAs system with 10 at-% As at 600C. Find the fraction of this system that is solid

I know how to do this

13. Describe the crystal structure of Si and that of GaAs

Diamond FCC. This is basically a FCC structure with stuff in the middle. Observe! we got 3/2 bonds between all particles, depending on type. In reality there are 3 but in the unit cell the edge particles have 2/1 bonds. The middle stuff:

- Take a particle that connects the corners to the closest middle face-centred particles.

- Each one of the face-centred particles is connected to 2 of the previousle mentioned particles.

14. What is a likely cause for the formation of a volume defect in a crystal?

Local percipitates (≈ collection) of impurites/dopants.

Lecture 3

15. What is meant with epitaxial crystal growth?

Epi = On top **Taxi** = Growth
The idea is to build a layer of single crystalline (semiconductor) on top of a (semiconductor) substrate. Nota bene, with the same crystal structure, otherwise shit gets crazy.

16. What are the main differences between MBE and MOVPE?

MBE - Molecular Beam Epitaxi
Quite self-explaining. You use a beam of atoms/molecules to populate the surface. Most often III-V.
Properties:
- UHV (= Ultra High Vacuumchamber) system (clean)
- Elemental sources (clean)
- Source delivered to the surface through a beam
- Slow growth rate (good control)
- Best material quality (of the 2 options)

MOVPE - Metal-organic Vapor Phase Epitaxi
The book refers to this by MOCVD, a family name that includes other types than epitaxial film growth. Is based on the VPE-technique described by the following picture:

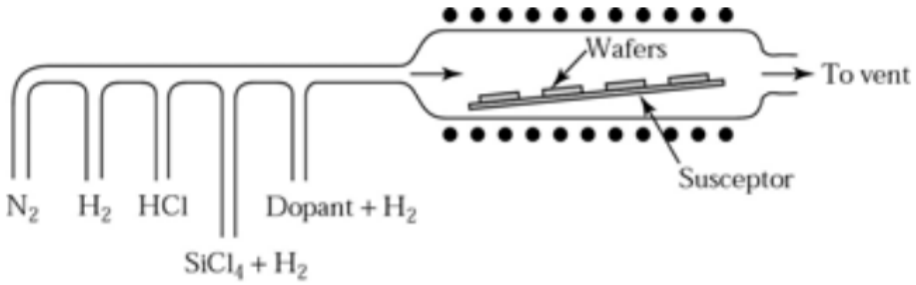


Figure 3:

Susceptor - A indirectly heated surface upon which the samples/wafers are placed.
Precursors → svenska → Föregångare
Back to the actual thing, **MOVPE**.
- It uses Metal-organic precursors that are easy to produce and handle.
- Used to grow layers of compund semiconductors (e.g. GaAs, InP ...)
- Allows a lower growth temperature than other non-organic sources
- Gives rise to complicated chemical reactions with rest producs.

Well back to the original question, what is the main difference?
It is that MBE is physically attaching an element/compound to the surface by beaming it towards it. Meanwhile, MOVPE is using vapour and chemical reactions to apply the given compound/element to the surface.

17. What do we mean by heteroepitaxy and homoepitaxy?

Homoepitaxi - Epitaxi and substrate layer are the same
Hetroepitaxi - Epitaxi and substrate layers are different

18. Can heteroepitaxy be lattice-matched?

...Yes? It is a good advantage to have so you do not get strains in a material.

19. An engineer wants to grow GaxIn1-xAs on an InP substrate. What value of x (the fraction of Ga and the fraction of In) is needed so that she can grow a relatively thick film without defects occurring?

Gotta find a table for this...

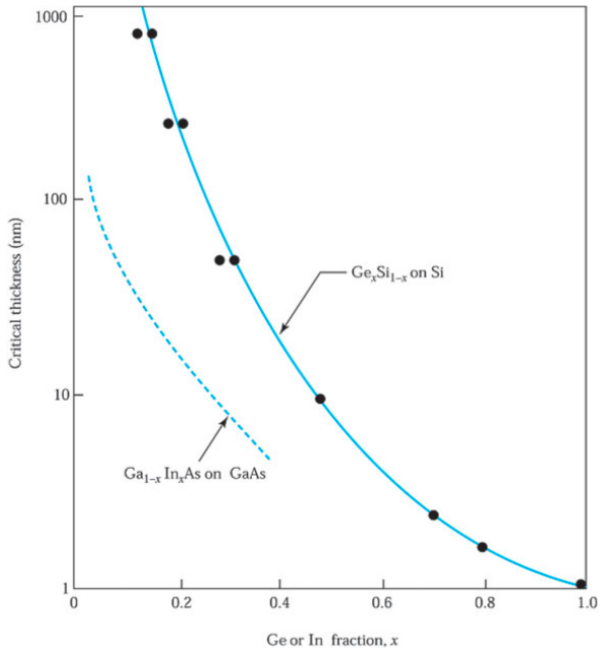


Figure 4:

So 100 nm is pretty thick. $x = 0.05$

20. Defects in epitaxial layers can severely degrade device properties. Can you describe at least three such kinds of defects and how to avoid them, if possible?

1. Stranski-Krastanow island growth
The epitaxial layer forms small island, or bubbles on the substrate.It is a lattice missmath, so you got to try to match the lattices better.
2. Anti-phase domains
This typical problem reveals itself when you are trying to have epitaxi of III-V (e.g. GaAs) on Silicon. Basically what happens is that the lattice diffrence strain pushes the GaAs around and therefore creates domains that have a higher concentration of one of the 2 than the other. Left picture down below. This can be solved by creating "steps" on the substrate that compensate for these lattice differences. Right picture below.

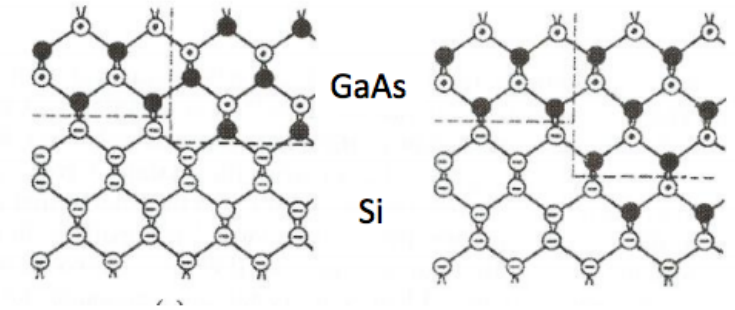


Figure 5:

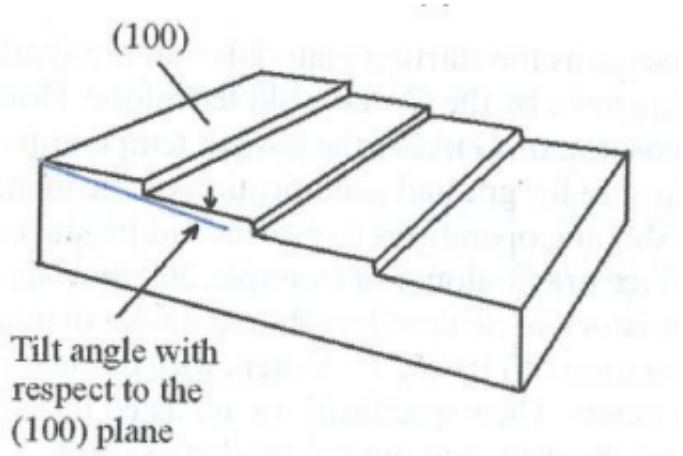


Figure 6:

3. Grain boundries and twin plane formations
Solution: increase diffusion length.

21. You have a heavily n-type doped GaAs substrate, but for some reason you want to have a 200 nm thick n-type low doped layer close to the surface. How can this be accomplished?

You use EBM or MOVPE to apply an extra layer and then let diffusion do it's magic. Maybe apply som heat aswell to catalyze the diffusion.

22. Why is III-V epitaxial growth on Si so important to industry? What problems are there?

Because III-V has high mobilty for chargecarrier, useful for building high mobility transistors and a direct bandgap, which makes them very usefull for building LEDs and solar cells. Unfortunately the wafer cost is extremely high. Using a silicon substrate would make the cost manageable. Problem? Anti-phase domains. Look at the questions above.

23. What is the purpose of a clean room beyond making sure that the environment inside isclean?

- Proper temperature and humidity
- Filtration of light that can damage the equipment, e.g. yellow rooms to avoid UV-light
- Some rooms are shielded from outside elektromagnetic rediation → no electronics allowed
- "Optical floors" makes sure there are no vibrations
- The work benches have holes in the (=perforated) to make the cleaner and safer to work on

24. Why are some materials "strictly forbidden" inside commercial semiconductor fab (=processing plant)?

Because som elements are extreamly contaminating to e.g. wafers. For example gold.

25. How are clean-room clothes different from regular clothes?

They cover every inch of you body (depending on the strictness of the clean-room) to avoid you from contaminating.

26. How are wafers handled in modern processing plants?

By machines. They are kept in their own mini-environment and atmosphere. They are transported in sealed boxes.

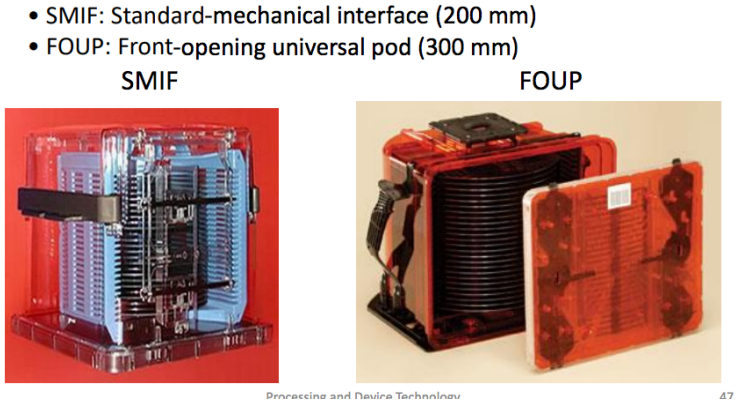


Figure 7:

Lecture 4

27. Outline the main parameters that describe the performance of a lithographic process.

1. Resolution, minimum feature size
2. Throughput, production frequency
3. Registration, Accuracy of the alignment of the litography

28. Which two parameters limit the resolution in shadow printing UV lithography?

1 and 3

29. Make a brief schematic outline of pattern transfer in optical lithography. Treat both positive and negative resist.

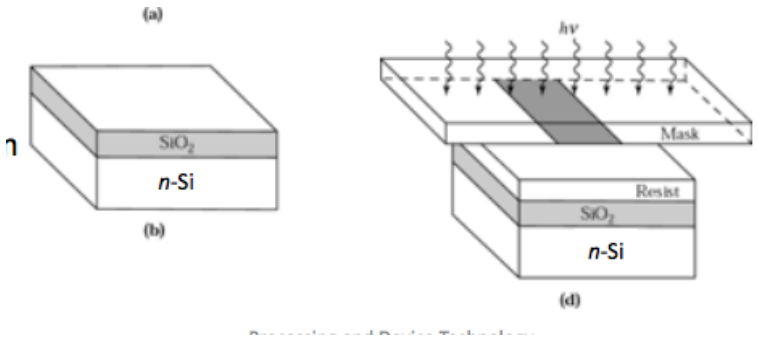


Figure 8:

If the resist is positive, the middle part will disappear. If negative, the outer parts.

30. Before application of resist one sometimes primes the semiconductor surface. Why?

SiO_2 is hydrophillic meanwhile the resist is hydrophobic (usually a polymer) and by priming the surfaces fits better together.

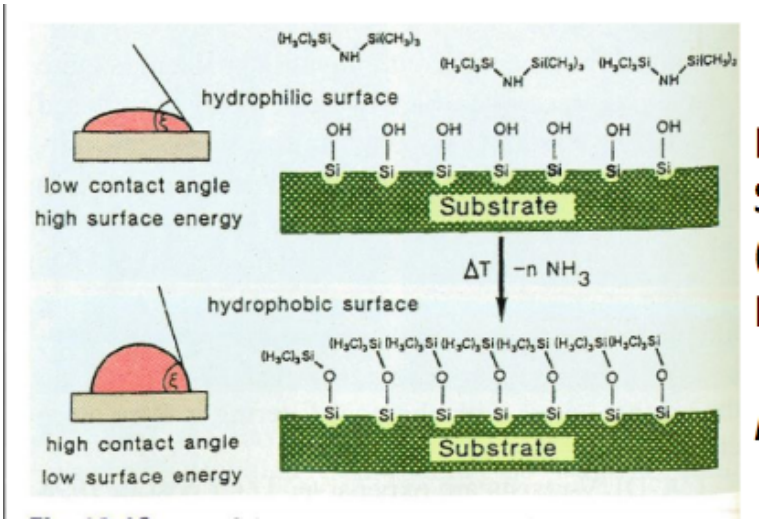


Figure 9:

31. Why is it especially important that the lithography is carried out in a clean room?

Because the whole sample can be destroyed if a small dustparticle ends up on the mask/between the mask and resist.

32. How does one normally apply the resist to the semiconductor substrate?

You place it on the substrate using a pipette then you spin i to get an even layer.

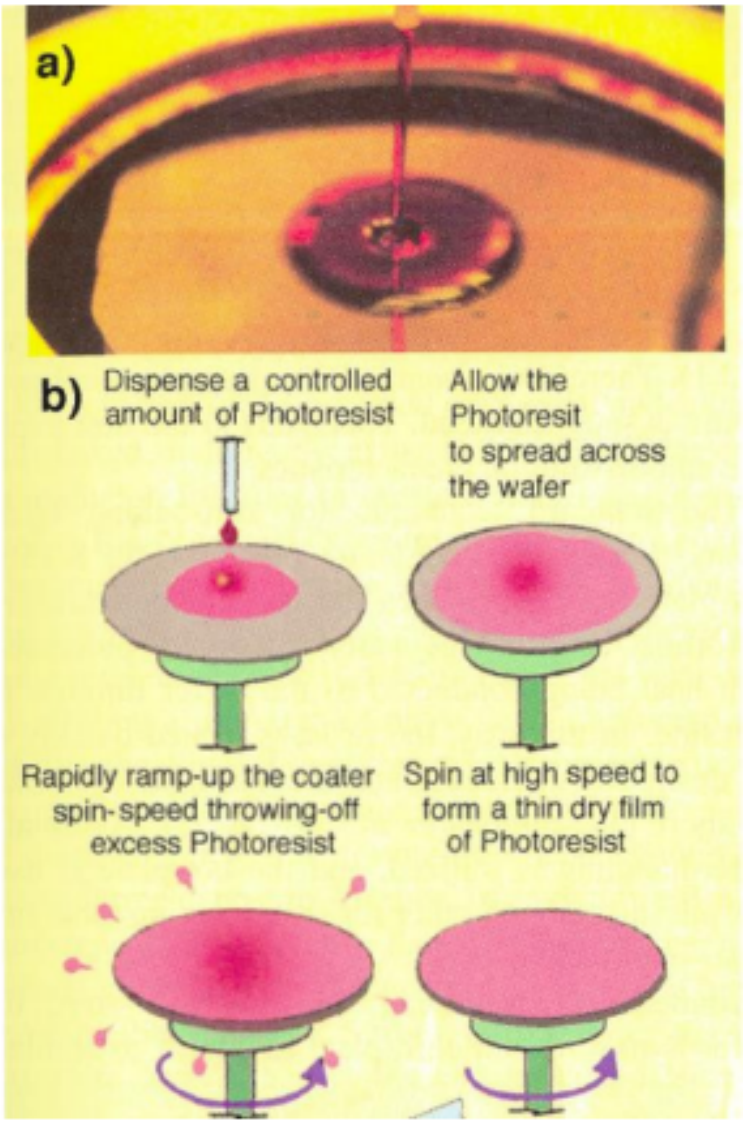


Figure 10:

The spinner usually starts spinning at a high speed in the beginning to throw of most of the resist and therefore create an even surface ($<$ 1s). The viscosity of the film increases with thinness and causes the solvent to evaporate. Typically after 30 s the film has stabilised.

33. Mention two important factors which determine the thickness of the resist layer in the resist deposition/application process.

1. Speed 2. Viscosity

34. Describe the lift-off process. Is there an alternative to the lift-off process to form, for example, an area of metal on a wafer?

You add chemicals that dissolves LOR (=Lift off Resist). Metal? Picture:

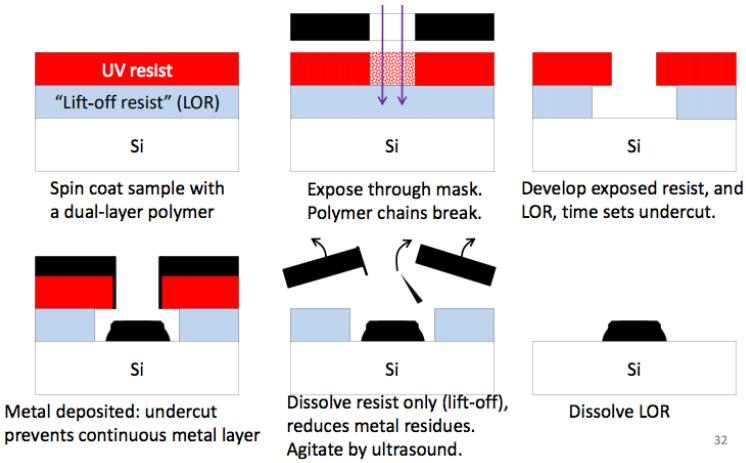


Figure 11:

35. The lift-off process does not work well if the deposited metal film is thicker than the resist. Why? (Make a sketch!)

Look at the picture on the previous question. If the mass of the metal is greater the agitated metal will only go off when the energy is enough to pull all of the extra material from the substrate off.

36. Describe some unconventional techniques that can push the resolution of UV-lithography beyond the wavelength of light used in the process.

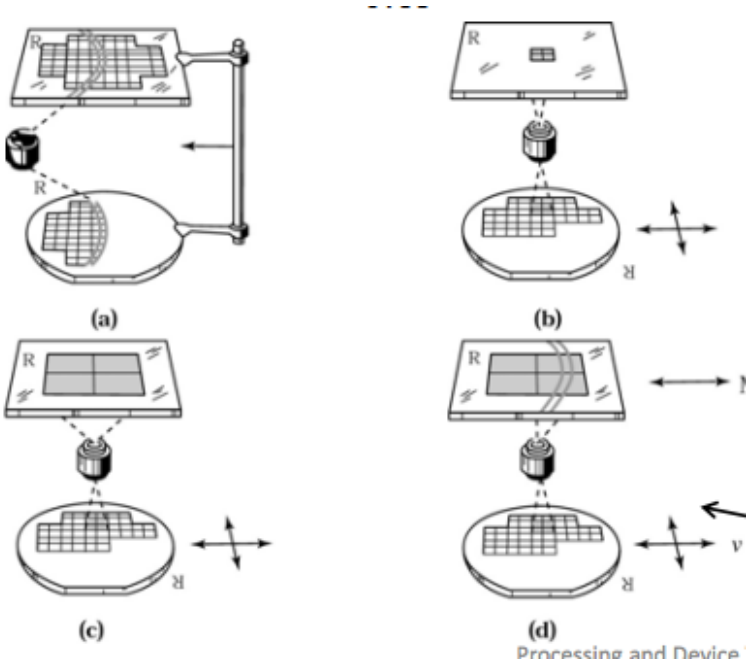


Figure 12:

(a) Annual field wafer scan - scanning the focal point at the lens while moving the template
(b) 1:1 step and reapeat
(c) M:1 reduction step and repeat
(d) M:1 reduction step and scan - combining (a) and (c)

37. What do you think will be the main limitation when developing future lithography systems?

Quality of the lenses. All the theories behind lenses and thier focal point etc is based on approximations and the "straight-line"-way of looking at light. This will start to become evident with smaller and smaller applications.

Lecture 5

38. Which are the two major techniques for thermal oxidation of Si? – Write down the respective reaction formulas and make a comment on the oxidation rates.

Dry Oxidation -
A slow process that creates thin high quality oxides. Very slow process

$$Si(s) + O_2(g) \rightarrow SiO_2(s)$$

Wet Oxidation -
Faster process that creates thicker oxides.

$$Si(s) + 2H_2O \rightarrow SiO_2 + H_2$$

39. The linear-parabolic model for Si oxidation is often written in the form: $x^2 + Ax = B(t + \tau)$. Consider the cases of x being either small or large - why is this model called linear-parabolic?

τ is the term to account for previous growth of an layer of oxide.
x is large $\rightarrow$ Ax term is insignificant $\rightarrow$

$$x^2 \approx B(t + \tau)$$

x is small $\rightarrow$ x^2 term is insignificant $\rightarrow$

$$x \approx \frac{B}{A}(t + \tau)$$

Comment: When is x big or small? Nobody knows. Why is it called linear-parabolic?
I guess because it is parabolic when x is large and linear when x is small.

40. Discuss why SiO_2 has been so important to IC-fabrication (think about the properties of SiO_2).

Because it is very easy to fabricate from pure silicon and it does not create any crystal-defects. It has a very large bandgap which makes it a good insulator.

41. Why is it not possible to thermally grow crystalline SiO_2 on a crystalline Si surface?

Because SiO_2 is amorph

42. Discuss some methods to determine the thickness of SiO_2
(and other dielectrics in general).

- Colour Inspection:
Very crude, you look at the colour and get an approximate thickness. Picture:

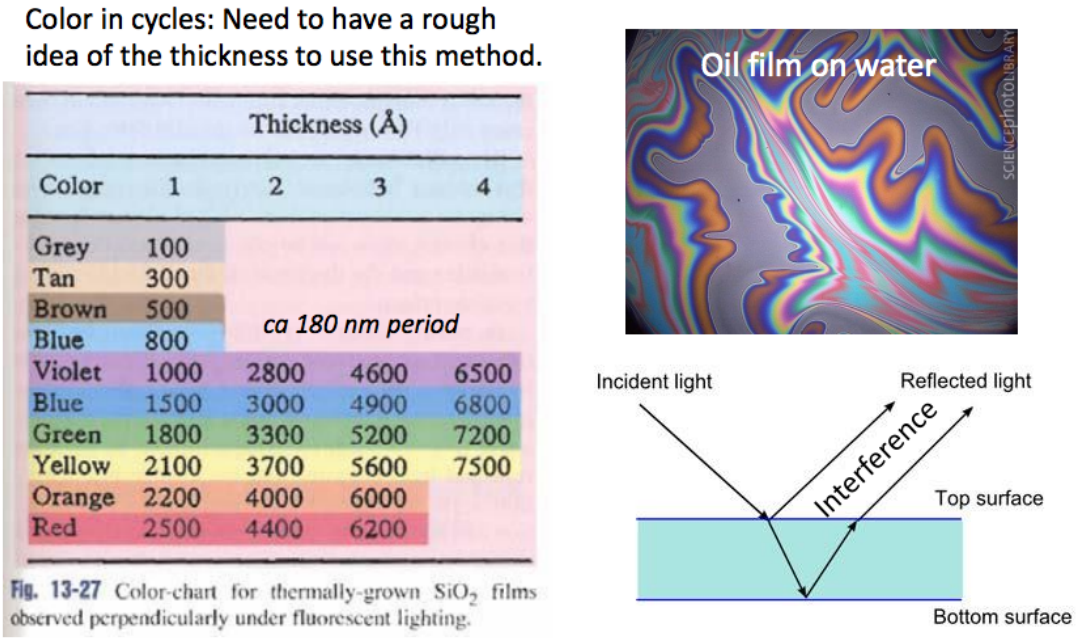


Figure 13:

- Interferometry optical:
You beem the sample with light and then you observe the wavelength that is returning.

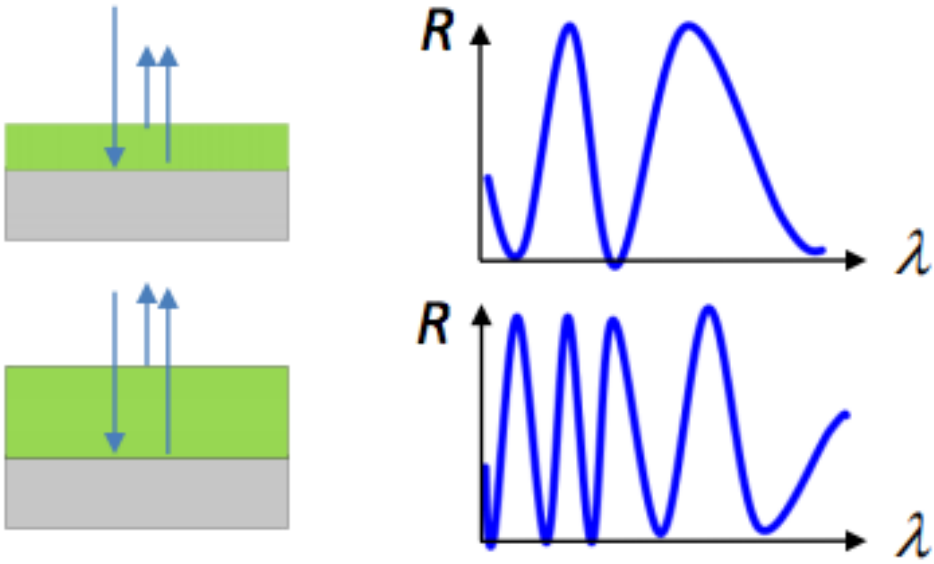


Figure 14:

- Ellipsometry:
You beem the sample with polarised light and observe the elliptical light returning. Than you compare the result with expected for the thickness of the SiO_2 and by iterating the program you receive the correct thickness.

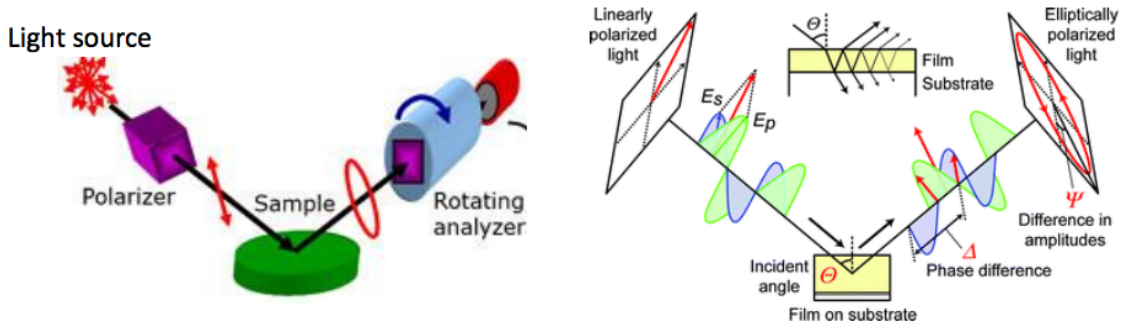


Figure 15:

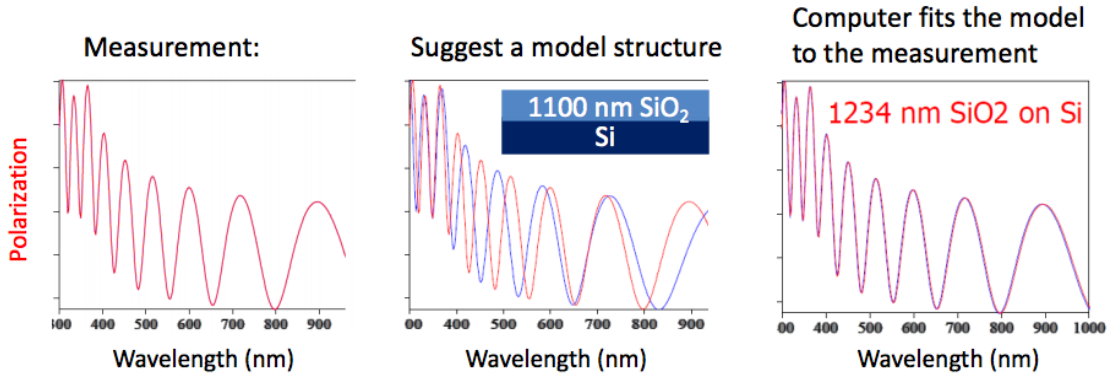


Figure 16:

- Profilometry:
Basically a AFM.
- Inspection of cross-section by high-resolution electron microscopy:
It does not say more than that it is very complicated in the powerpoint.

43. What measurement technique is typically used to determine the quality of a Si-SiO_2 interface (in terms of electron traps etc)?

A probe station. Works basically as a AFM.

44. In MOSFETs, which carrier type (holes or electrons) are close to the gate in the on- and in the off-state for pMOS and nMOS respectively? (4 cases)

For p-MOS:

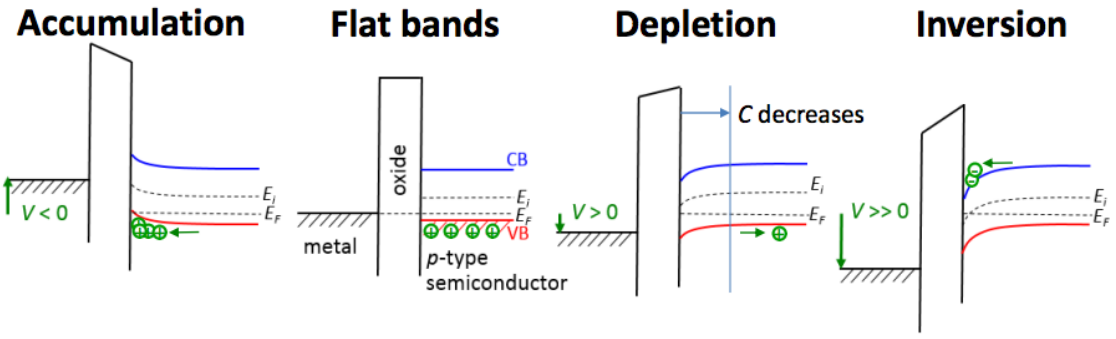


Figure 17:

n-MOS is just inverted.

45. What is meant by CMOS, and why is CMOS considered to be a low power technology?

A circut-schedule involving both a n-MOS and p-MOS. It is low power because the current never flows to the earth. Picture:

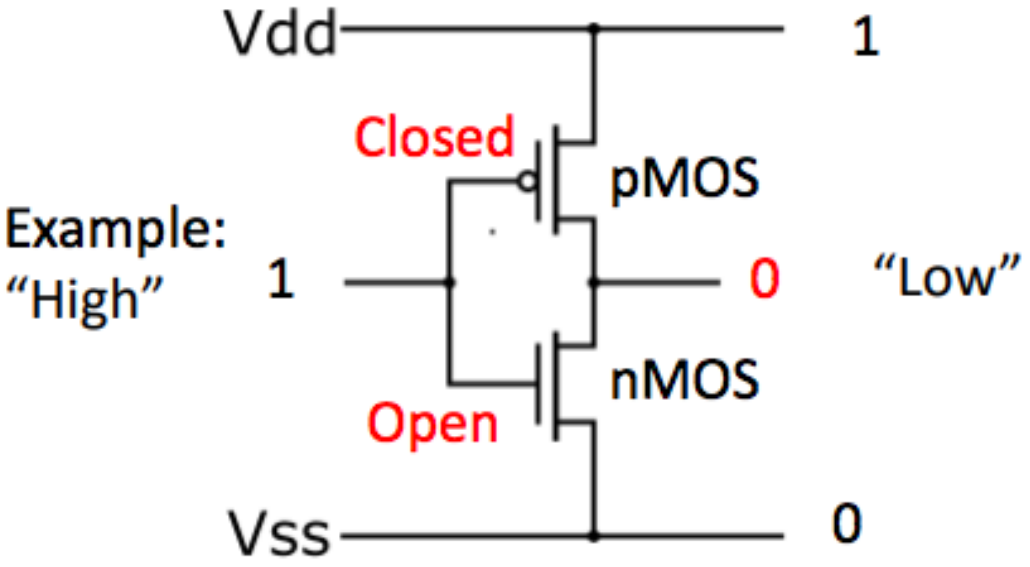


Figure 18:

Lecture 6

46. What are the main usages of deposited dielectric films?

- Insulation between metal layers (typically C- or F-doped)
F-doped - Fluorine doped
C-doped - Carbon doped
- Mask material for ion implementation and diffusion
Mask that can block a beem of ions, or blocks diffusion. - Final passivisation layer (typically p-doped)
- Diffusion source for Si-doping (usually doped with P, As and B)

47. Describe what happens in a typical CVD process.

CVD - Chemical Vapor Deposition
Basically we have chemicals in a gas that is deposited as a thin film on the surface. Ideally the reactions are only taking place on the wafers surface. The reactants are gases and the product is a thin film. Activation energy is needed.

48. What are the advantages, and potential disadvantages, with a plasma-enhanced CVD process?

Advatages -
- Lower disposition temperature possible
- Amorphous solid-deposition
- Deposition can be combined with pre-plasma etching
Disadvantages -
- Often significant impurity incoporation, a lot of hydrogen usually
- Complements but do not replace thermally grown SiO_2, it has worse quality

49. What is the general trend in the quality of deposited SiO_2 with decreasing deposition temperature?

Higher temperature → Better/more pure thermally grown SiO_2
Note Bene, Too high of a temperature may destroy the existing structure.

50. What is meant by conformal and non-conformal step coverage?

Conformal step coverage -
Uniform thickness. Usually desired. This happens because of the fast migration of reactants.

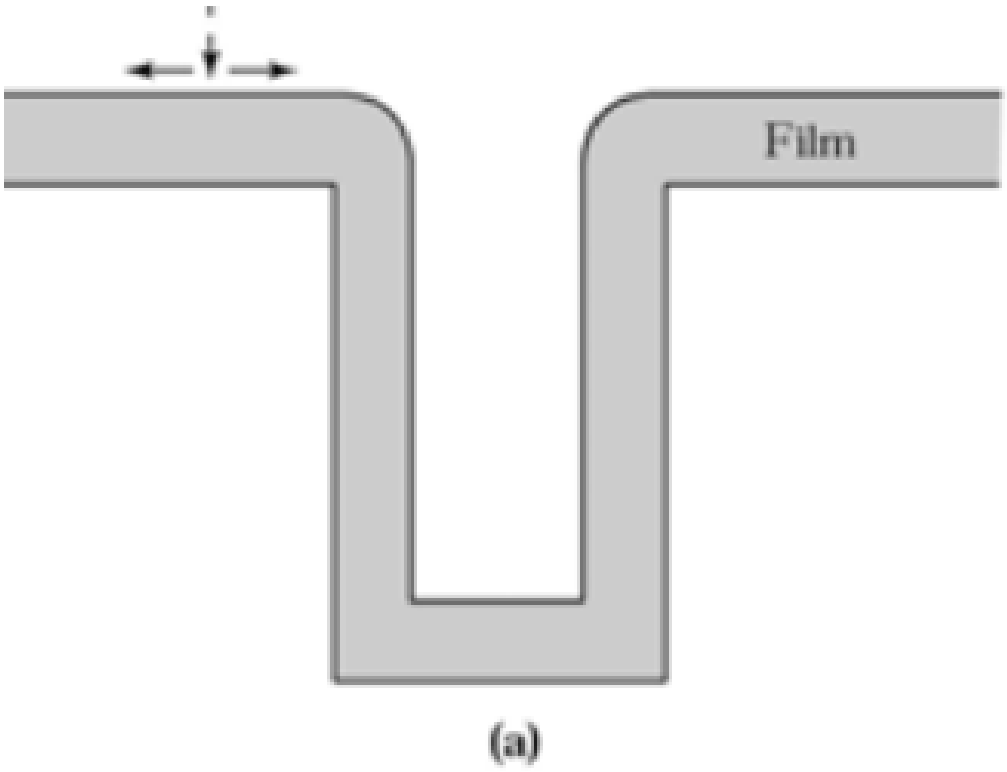


Figure 19:

Non-Conformal step coverage -
Non uniform thickness. When the reactants absorb and react with little or no surface migration.

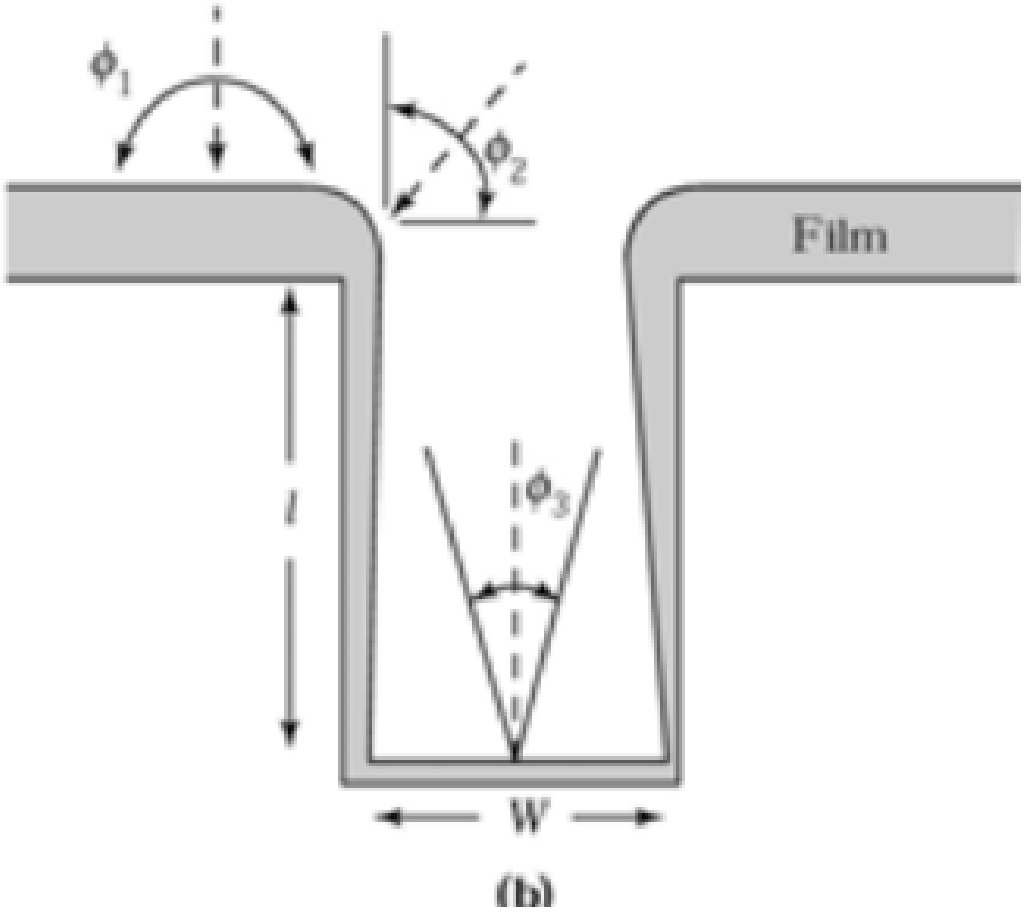


Figure 20:

51. Why would one want to have low dielectric constant materials as insulation material between the metal interconnect layers?

Dielectric constant $\rightarrow \kappa = \epsilon_r$. κ is frequency dependant. If non is given, assume $\omega = 0$.

$$C = \epsilon_r \epsilon \frac{A}{d}$$

Therefore
high $\kappa \rightarrow$ High capacitance
low $\kappa \rightarrow$ low capacitance
Now, which structures are desired to have what?
Low κ -
- Insulation and passivisation of devices and IC
- Insulate multilevel-metallization $\rightarrow$ Reduced RC-constant **High** κ -
- In gate oxides and DRAMs $\rightarrow$ high capacitance and low leakage

52. What can be done to SiO_2 to lower the dielectric constant?

1. F-doping
2. C-doped
3. Porouse SiO_2, closer to vacuum you know...

53. Where is a high-κ dielectric desirable, and why?

Insulation at the gate, to avoid voltage leakage and at DRAMs, an structure that is used to story memory. It is basically a capacitor, the higher $\kappa \rightarrow$ the better capacitor.

Lecture 7

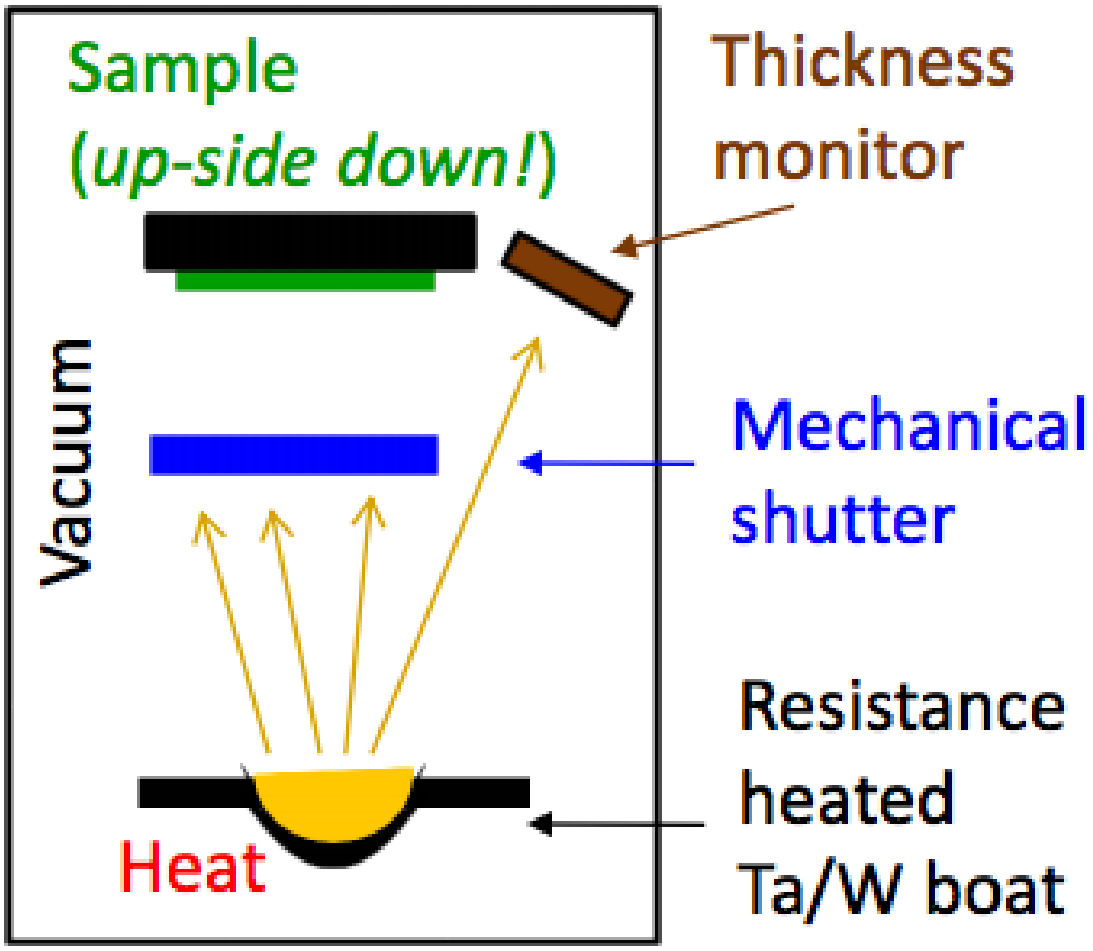
57. For metal deposition we can use CVD and PVD processes.
Explain what we mean by the distinctions: chemical and physical.

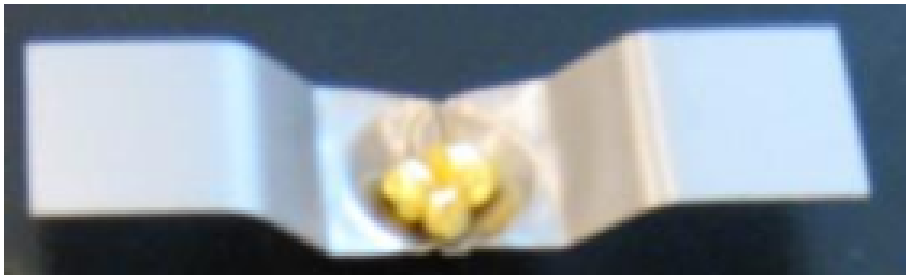
Chemical is referring to the fact that the deposition is a chemical process that includes reactions, reactants, catalysts and products. Meanwhile the **physical** is referring towards that there are practically no reactions taking place, simplified you are just building an metal layer with "bricks".

58. PVD can be divided into basically two main directions:
evaporation and sputtering. Explain both these processes so
that a fellow student who has not taken this course would understand.

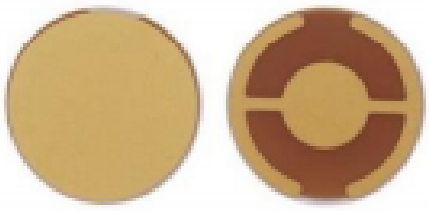
Evaporation -
You have the sample "in the ceiling" and you evaporate the desired metal so that it is transferred towards the sample. Note that the metals trajectory is in straight lines. Because of this, the step coverage is bad. The metal lump that is the source of the evaporation is fittingly called, "the source". The source is melted by one of these techniques:
- Resistance heating: Having a current running through the source/container
- RF heating
- Focused electron beam

The sample is not heated which results in little or no diffusion. The thickness of the deposition is monitored by the change of resonance frequency of a quarts crystal.





Au: Melting point: 1060 °C



Piezo-electric quartz crystal detector

59. The melting temperature for pure Al and for pure Si
is higher than the melting temperature for Si-Al alloys.
What characteristics is such a system said to obey?

Junction spiking -
During contact anneling, Si dissuses into Al and leaves holes for Al to fill. If the holes are prevelent deeper then the underlying n-doped area the pn-junction will not work. Look at this picture:

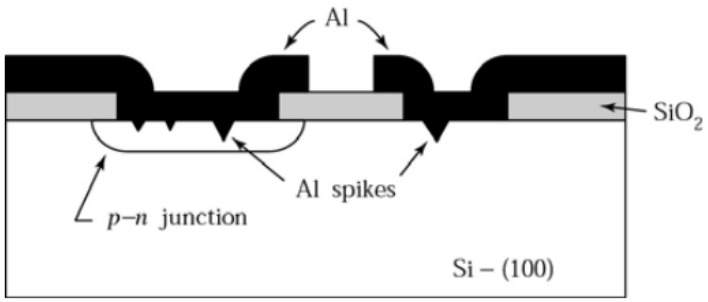


Figure 22:

So basically Al atoms leak down into the n-doped area and destroys it.

To avoid this, Add Si to Al when deposeting it, saturate it or/and introduce an small barrier of TiN between the Al and n-Si.

60. The solid solubility of Si in Al is quite high.
Describe the problem (or problems) that this could lead to
if Al and Si is used in combination

- Unintentionally p-doping Si
- Junction spiking.

61. Describe the process of electromigration, and what it can
lead to in a conductor

The electrons momentum can push around the nucleus, and therefore destroy the connection/cable

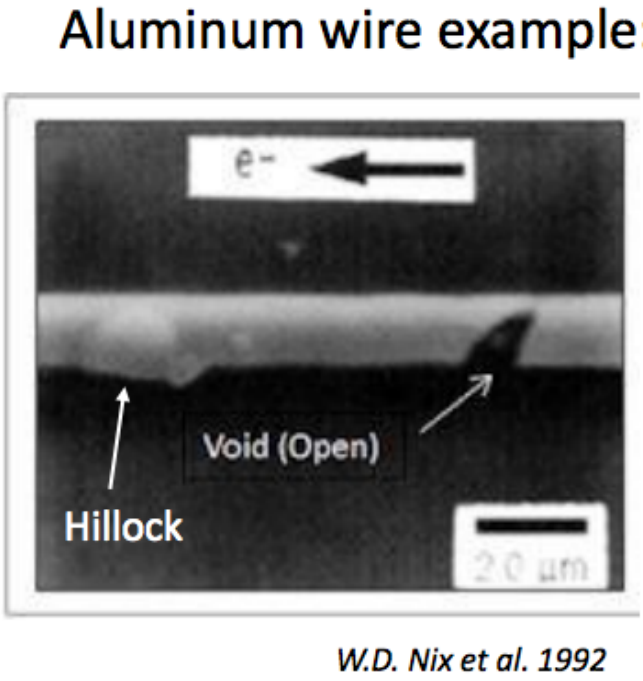


Figure 23:

62. Name and describe a copper interconnect process, which does not require etching of copper. Which process is used instead of etching the copper?

Electroplating -

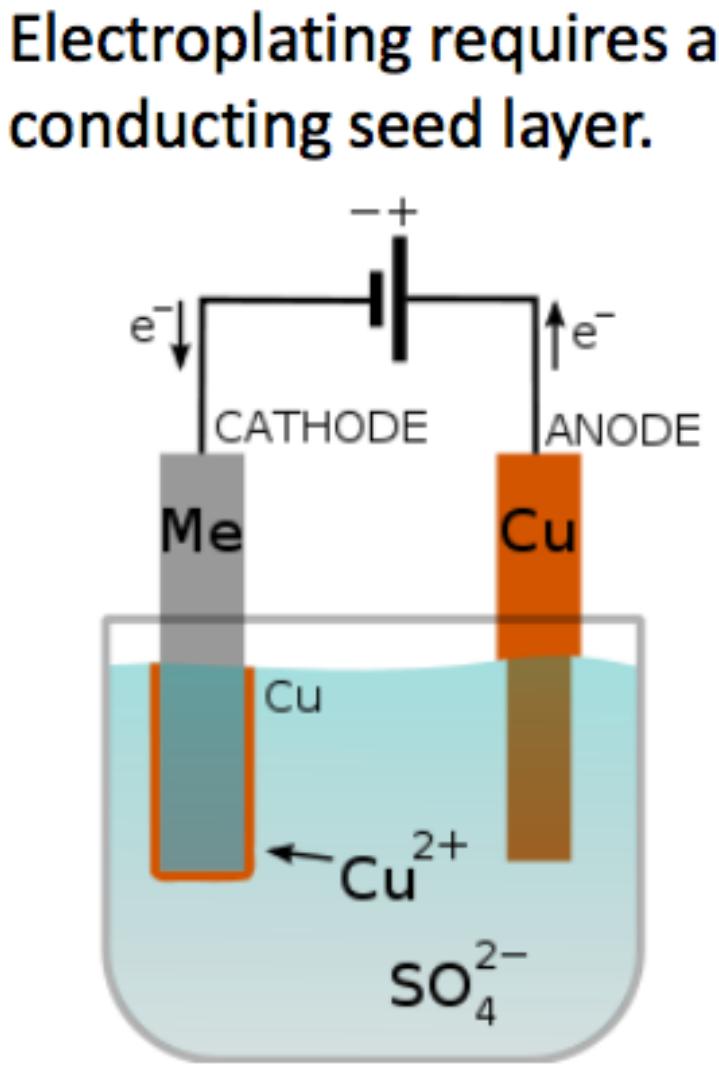


Figure 24:

The damascene process -

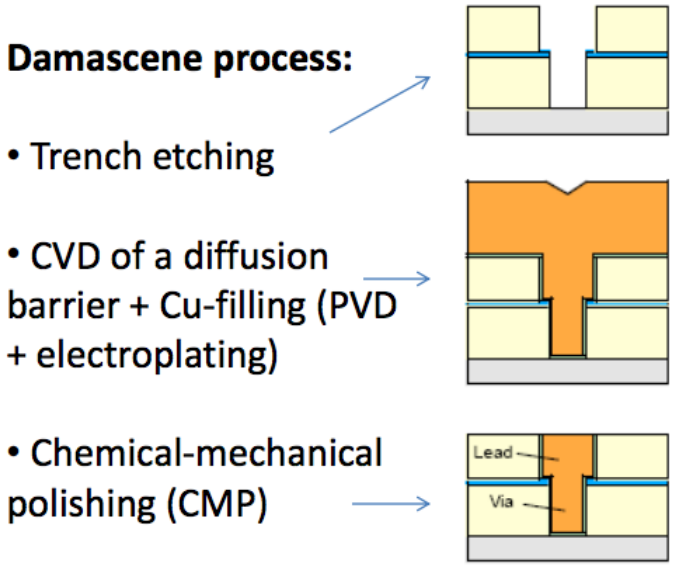


Figure 25:

Where CMP - Chemical Mechanical Polishing is

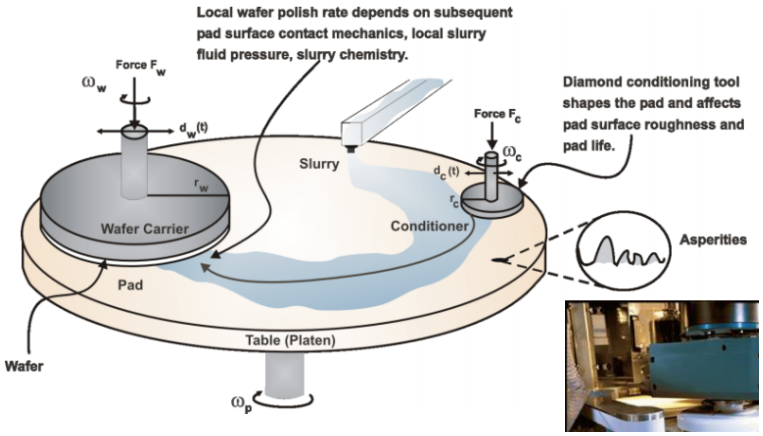


Figure 26:

wafer is held on place using vacuum and it is rotated and polished using nm-sized abrasive particles (silica).

63. How is sheet resistance defined? A 10 μm long and 0.2 μm wide metal line has a sheet resistance of 7 ω/square. Calculate the resistance of this metal line

$$R = \rho \frac{L}{TW}$$

Where T is the thickness, W is the width, L is the length and ρ is the charge density. If $L = W \rightarrow R = \frac{\rho}{T}$, unit: ω/square. Towards the question $\rightarrow$

L = 10 μ m, W = 0.2 μm,

$$\rho = RT =$$

64. What is a silicide?

An silicon alloy. Usually conduct better than pure Si. Used to reduce resistance.

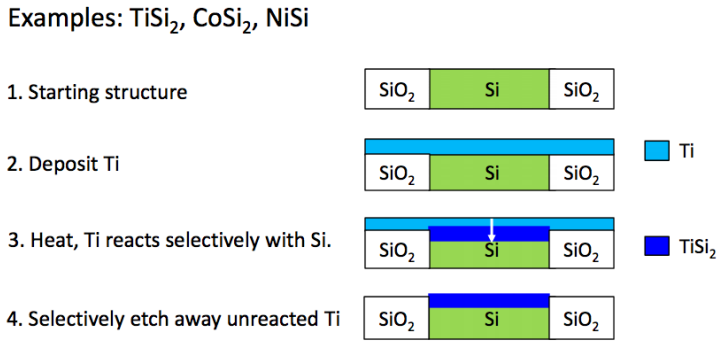


Figure 27:

65. Try to recreate a mind map of various thin film deposition techniques, based on (for example) the state of the surrounding medium.

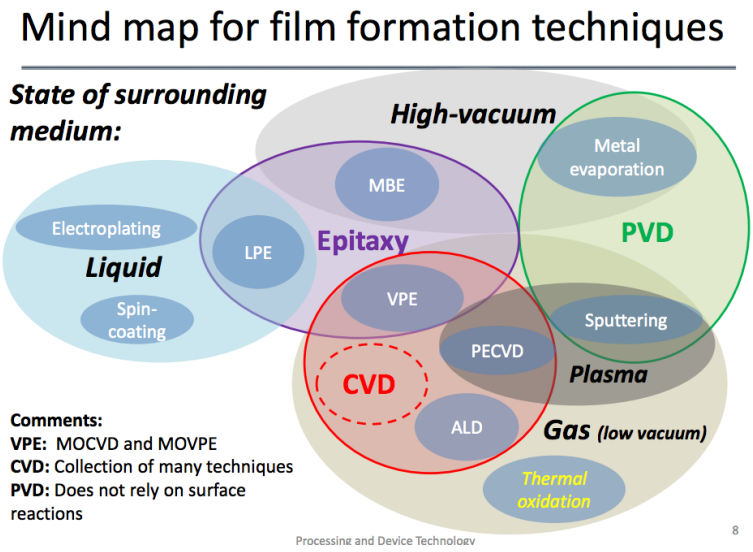


Figure 28:

66. Why is not a physical mask necessary in electron beam lithography? How is the exposure done?

Because you can just aim the electron beam.

67. How does the throughput of electron beam lithography compare to UV lithography?

Very low

68. What is meant with "proximity effect"?

An area in proximity to another target area are getting more exposed than others. E.g

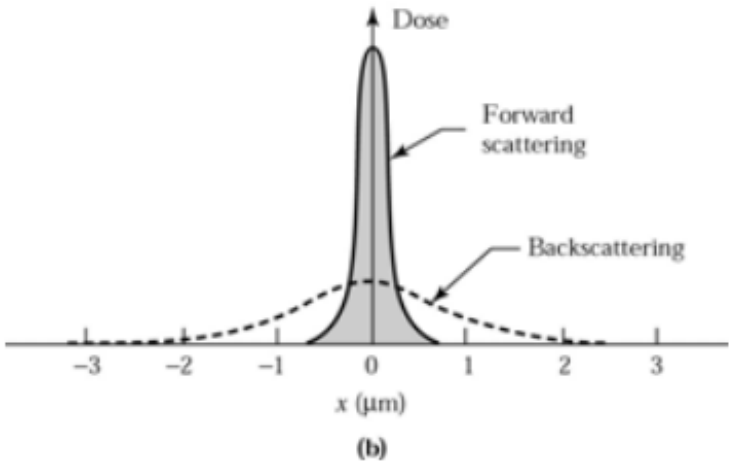


Figure 29:

69. Briefly outline the nanoimprint lithography (NIL) process.

Basically a stamp.

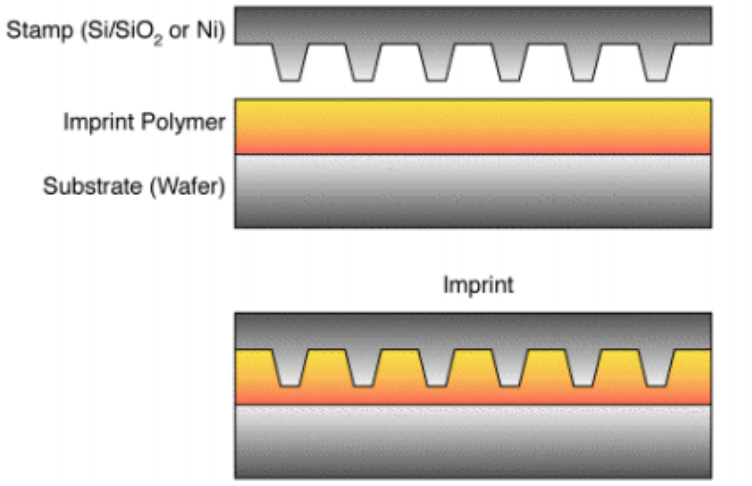


Figure 30:

Lecture 8

70. Why is reaction-limited etching as opposed to diffusion-limited etching preferred in semiconductor device processing?

71. Wet chemical etching consists of two major steps: oxidation (or reduction) and dissolution of the reaction products. Which chemicals are normally used to etch Si and what are the roles of these?

1. Oxidation -
HNO_3
2. Oxide Dissolution -
HF

72. How do you etch SiO_2? – Compare with Si etching.

Since it is already oxidised you only need step 2 → HF.

73. Most wet etchants are isotropic, which is a problem in pattern transfer. What does isotropic and anisotropic mean? **Isotropic** → Even, **Anisotropic** → Uneven

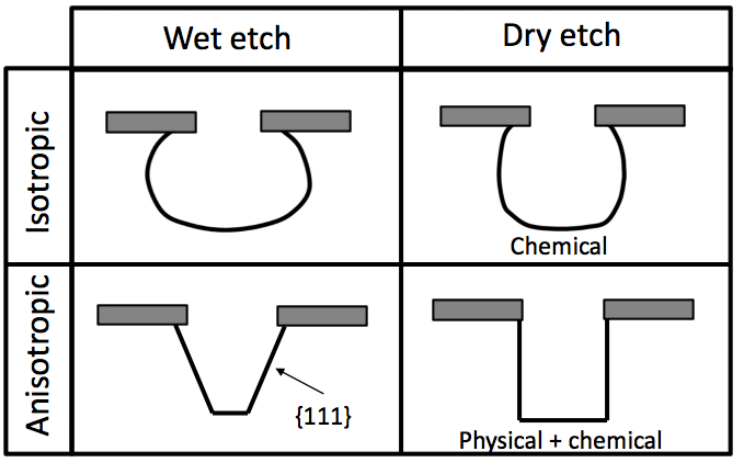


Figure 31:

74. Give an example of an orientation dependent (wet) etchant of Si.

KOH, Water and Isopropyl Alcohol

75. Explain the concept of selective etching.

H_2SO_4:H_2O:H_2O etches InGaAs and InGaAsP but not InP
HCL:H_2O etches InP but not InGaAs and InGaAsP

76. What is a plasma, and how can it be formed?

Plasma is a cloud so hot so that some of the electrons have been separated from the nuclei.

77. What does a plasma offer in a dry etch process?

The plasma has 2 roles:
1. Generate charged ion to get physical etching
2. Generate radicals in a reactive gas

78. Dry etching can be dominated by physical or chemical processes. What do we mean by physical and chemical?

Done this before brah

79. Think of a reactor configuration
(A: type of gas, B: pressure, C: electrode layout)
that gives rise to physical etching, and a corresponding configuration
that instead gives chemical etching of a polymer/organic film.

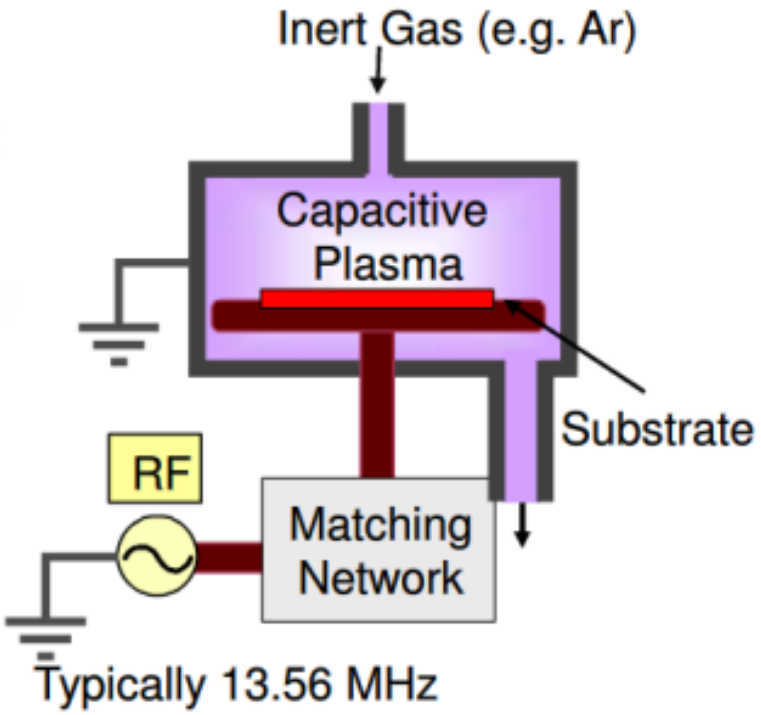


Figure 32:

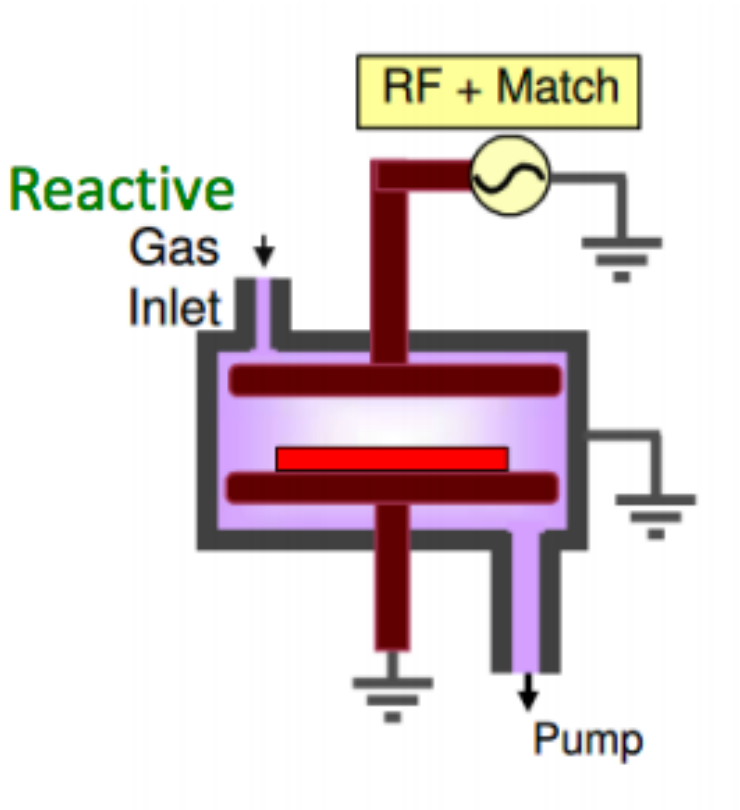


Figure 33:

80. The advantage with physical dry-etch methods is that they give anisotropic etch profiles. Describe an etch method, which still generates anisotropic etch profiles but gives rise to less bombardment induced damage.

Plasma

Lecture 9

81. Write Fick's first law and explain the minus sign.

F=-D$\frac{\partial C}{\partial x}$, Where F is the flux, C is the concentration, x is the dimension which the diffusion is happening in and D is the diffusion constant. The minus sign is because the increasing change results in a lower flow because of the fact that the particles disappear.

82. Write Fick's second law in one dimension – both for the general case and for the case when the diffusion constant is concentration independent.

Independant:

$$\frac{\partial C}{t} = D\frac{^2C}{\partial x^2}$$

For the situations where D is dependant of x, $D = D_S(\frac{C}{C_S})^\gamma$, index s = surface, $\rightarrow$

$$\frac{\partial C}{t} = \frac{\partial}{\partial x}[D_S(\frac{C}{C_S})^\gamma \frac{^2C}{\partial x^2}]$$

83. Assume that the diffusion constant is independent of concentration (intrinsic diffusion). Write down the solutions to the diffusion equation (Fick's second law) for the two special cases brought up in the course. In addition, also give a brief explanation of these cases

2 cases:
1.**Pre-desposition**:
That you have a constant concentration of dopants. Boundry conditions:

$$C(t,0) = 0, \text{At the beginning, the concentration is zero everywhere}$$

$$C(0,t) = C_s, \text{The concentration is constant at the top}$$

$$C(\infty,t) = 0, \text{At "very far away" the concentration is 0}$$

$\rightarrow ... \rightarrow C(x,t) = C_s(1 - erf(\frac{x}{2\sqrt{Dt}}))$ 2. **Constant total dopants**:

$$C(x,0) = 0$$

$$\int_0^\infty C(x,t)dx = S$$

$$C(\infty,t) = 0$$

Math gives $\rightarrow$

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} e^{\frac{-x^2}{4Dt}}$$

84. Say that you know the background doping concentration (p-type) and you want to make a pn-junction by diffusion with donor atoms. Describe (in words and equations) how you would calculate the junction depth.

The junction depth is defined as the diffusion depth. This is described by the term $\sqrt{Dt}$. You get this by calculating the errorfunction.

85. Discuss the two-step diffusion process carried out in IC-fabrication where these two special cases are relevant.

You use both of these methods. First pre-desposition and then drive-in

86. What happens to the surface impurity concentration in doped Si during Si-oxidation in case impurities (dopants) diffuse fast in SiO_2?

The dopants will be redistributed when the silicon is oxidized. The equalibrium number is different in this case $\rightarrow$

$$k = \frac{\text{impurity conc. in Si}}{\text{impurity conc. in } SiO_2}$$

87. When impurities are diffused into the semiconductor through masks, lateral diffusion takes place at the mask edges. Draw a figure that explains lateral diffusion and discuss potential negative effects from it.

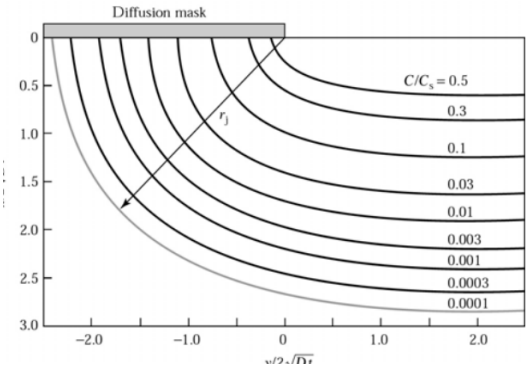


Figure 6.12 (p.119) Diffusion contours at the edge of an oxide window; r_j is the radius of curvature.

Figure 34:

It may penetrate in areas with higher curvature. 88. What happens to Fick's second law when impurity-related vacancies
dominate over the intrinsic vacancies? Is the Diffusion coefficient
then higher or lower?

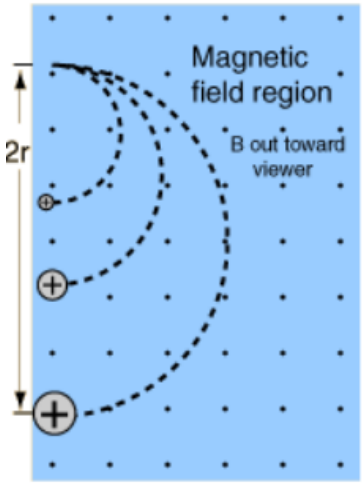
88. What happens to Fick's second law when impurity-related vacancies dominate over the intrinsic vacancies? Is the Diffusion coefficient then higher or lower?

Lower, because of a higher concentration.

Lecture 10

89. The mass analyzer in an ion implanter functions as an ion sorting tool that "decides" which ions that may take part in the implantation process. By which principle(s) does it work?

It sorts the ions according to the formula below, basically sorts it by how much it trajectory is changed by the magnetic field.



Mass analyzer:

$$r = \sqrt{\frac{2mV}{qB^2}}$$

m: ion mass
q: Ion charge
V: Ion acc. Voltage
B: magnetic field

Figure 35:

90. Define range and straggle. – However, the quantities you use in calculations are projected range and projected straggle. Define these quantities. Are they smaller or larger than the (unprojected) range and straggle, respectively?

I have no idea but I am guessing that it can be longer due to ion-channeling.

91. Write down the ion distribution function and explain the included quantities

$$n(x) = \frac{S}{\sigma_p\sqrt{2\pi}}\exp(\frac{(x-R_p)^2}{2\sigma_p^2})$$

Approximately an normal distribution. R_p is the projekted range, σ_p is the projected straggle → statistical fluctuation, se the picture:

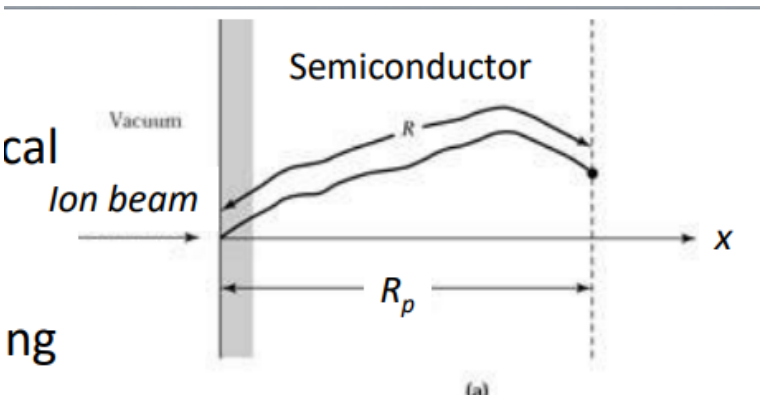


Figure 36:

S is the dose of ions per unit area.

92. Describe the two stopping mechanisms for ions.

1. Coulombic interactions with the nuclei -

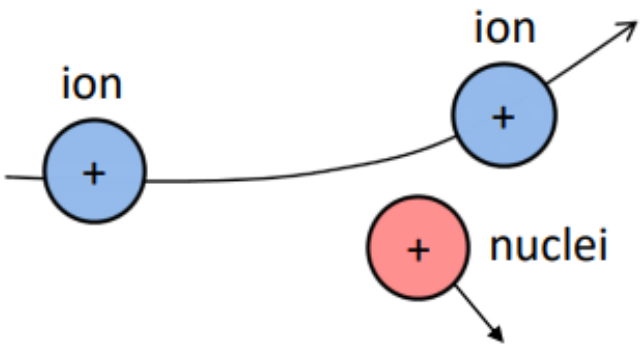


Figure 37:

Basically crashes/interacts with the nuclei of the material. 2. Coulombic interactions with the electrons -

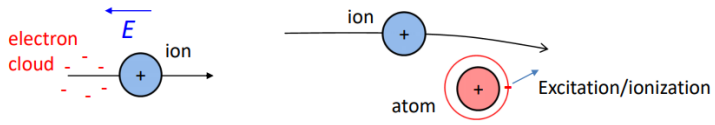


Figure 38:

Either the elctrons interact with the ion while they are orbiting the atom or they are forming a tail slowing the ion down.

93. What is ion channeling and what does it lead to?
Which measures can be taken to reduce it?

When ions "align with the mayor crystollographic direction". Basically the crystal has a structure that builds a tunnel for the ions. Picture:

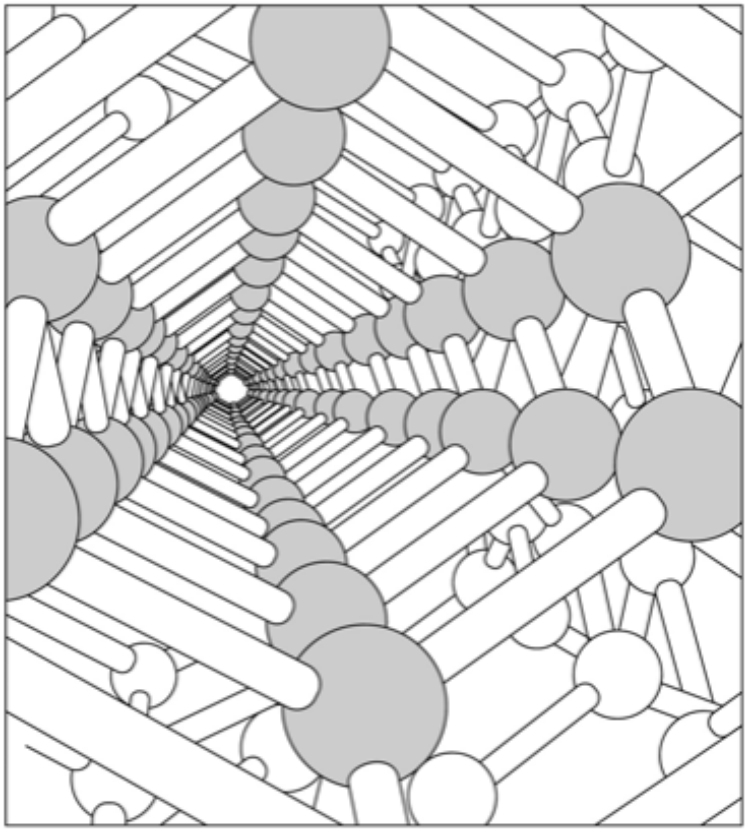


Figure 39:

94. Say that you know the background
doping concentration (p-type) and you want to make

a pn-junction by implanting ions that would give n-type doping.
Describe (in words and equations) how you would
calculate the junction depth.

Using the given equations I would calculate the concentration of the p-doping, add that much of n-doping, and then add n-doping so that the material is given the wanted charactaristics. Equations? No, I am lazy

95. The implantation disorders caused by
light and heavy ions are quite dissimilar. Explain how and why.
What does this disorder lead to in terms of semiconductor performance?
Can the affected semiconductor parameters be restored –
in that case, how?

Light → electronic damage in the start then nuclear far into the sample and Heavy → create an big dissorder cluster right in the beginning in the sample // Nuclear damage.

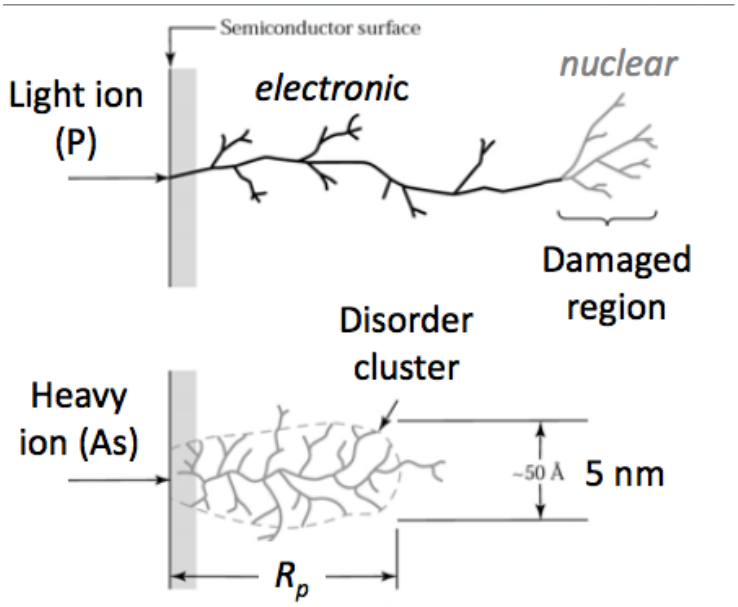


Figure 40:

96. How can an almost constant impurity profile over a
fairly large range be obtained in ion implantation?

By varying the energy of the beam/ions

97. Ion implantation is today used for most impurity
doping in CMOS (digital electronics) –
why? What are the advantages of ion implantation compared
to doping by diffusion?

You can control it more exactly creating an evenly distributed doping profile by varying the energy of the ions.

98. Describe some methods, both destructive and non-destructive, that can be used to evaluate doped materials in terms of impurity type/concentration and junction depth

There are four different ways to do it (according to the powerpoint):
1. **4-probe measurement**:
A current is passed between the 2 outer probes and a voltage measurement is taking place between the two inner probes.

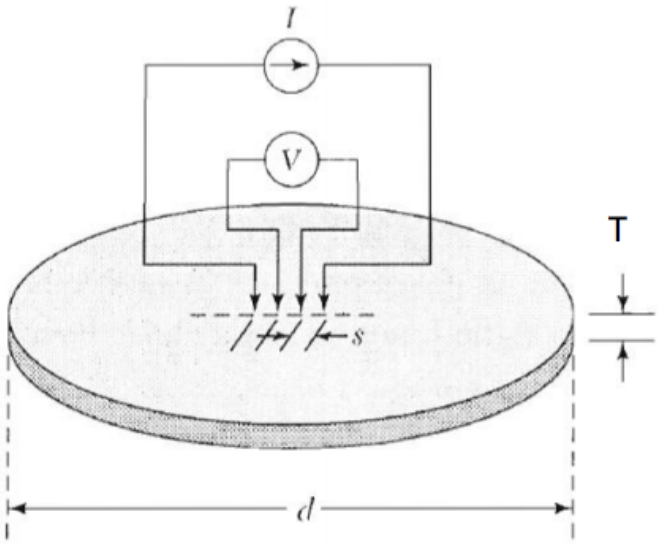


Figure 41:

This assumes the following:
A. The sample diameter, d, is very large (what is very large?)
B. Meanwhile the thickness, $T << d$, is very thin (what is very thin?)
C. Probes spacing is equal, everything is symmetrical at the figure above
2. **Spread resistance profiling**:
The sample is cut in an angle then two probes measure the resistance profile.

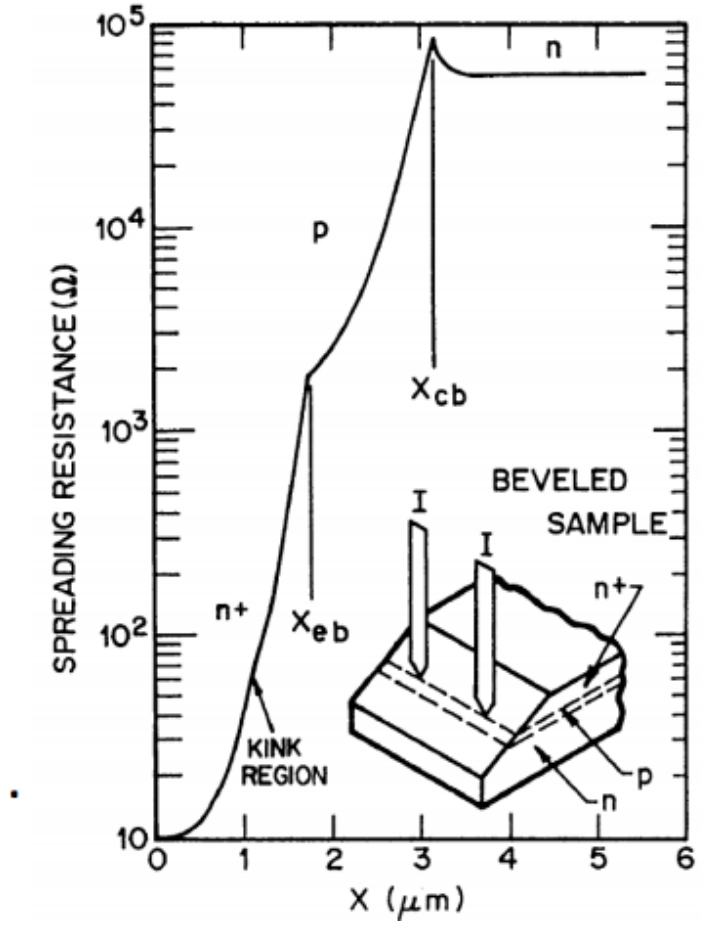


Figure 42:

This creates an high resolution profile of the carrier concentration but it only measures the electrically active dopants.It is also really fucking hard to do. It also destroys the sample...

3. **Secondary Ion Mass Spectrometry, SIMS**:

So you beam the sample with ions and look at what bounces of.

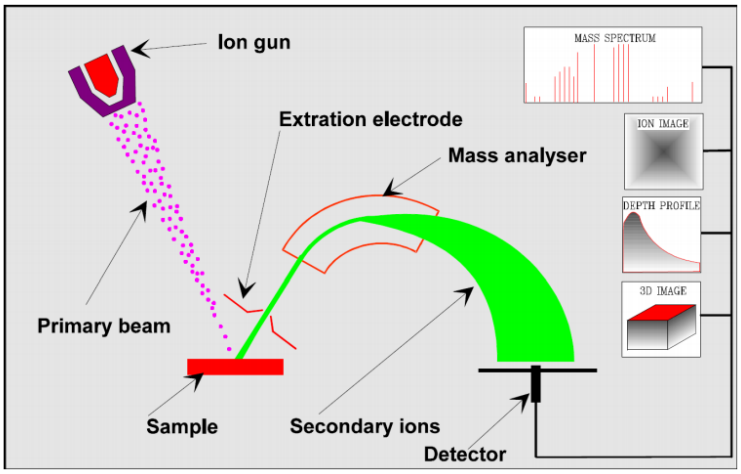


Figure 43:

So the ions who bounces of is analyzed according to a charge to mass ratio, kinda like the mass-analyzer in the ion-implanter. Observe, the ions CREATED by the beam are the intresting ones. The instument must be tuned to the different materials since the ionisation of atoms can be quite different. It has an high sensitivity and excellent depth resolution. It does not discriminate between active and inactive dopants, which is a problem.

Lecture 11

99. For CMOS-ICs down to 0.35 μm, LOCOS can be used to isolate active areas from each other. What does LOCOS mean? Describe the LOCOS process. Why do you think that LOCOS does not work for smaller scale ICs? Mention an isolation method that can be used for smaller ICs than 0.35 μm

LOCOS - **LOC**al **O**xidation of **S**ilicon, wiki:
"The main goal is to create a silicon oxide insulating structure that penetrates under the surface of the wafer, so that the Si-SiO_2 interface occurs at a lower point than the rest of the silicon surface. This cannot be easily achieved by etching field oxide. Thermal oxidation of selected regions surrounding transistors is used instead. The oxygen penetrates in depth of the wafer, reacts with silicon and transforms it into silicon oxide. In this way, an immersed structure is formed."

LOCOS does not work for smaller ICs because of the creation of the "Birds-Beak"

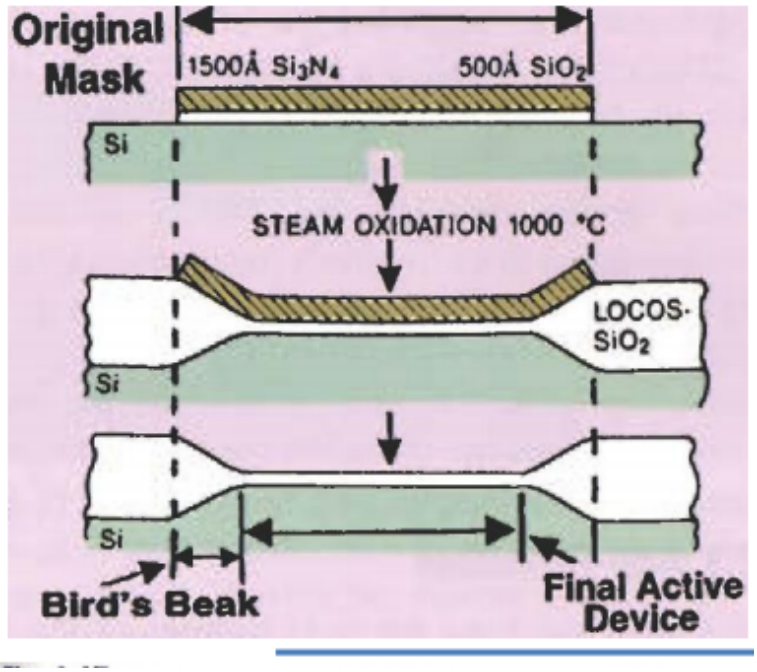


Figure 44:

Instead the **Shallow Trench Isolation** is used:

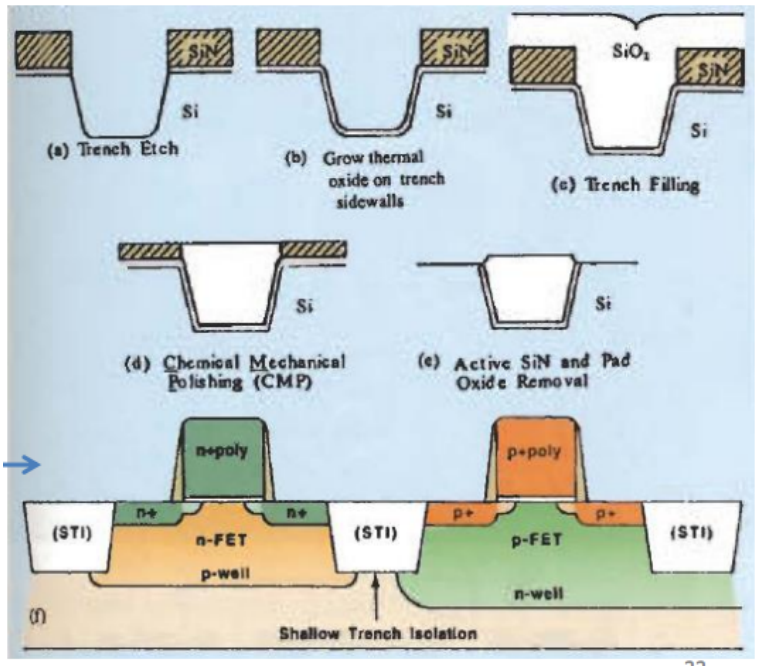


Figure 45:

100. Why is a SiO_2 gate oxide formed by dry

and not wet oxidation?

Beacuse we want a high quality oxide. It is easier to create a thin oxide with dry oxidation since it has a slower porduction rate.

101. What does salicide mean?
Describe the salicide process.

Salicide - **S**elf**a**ligned si**licide**

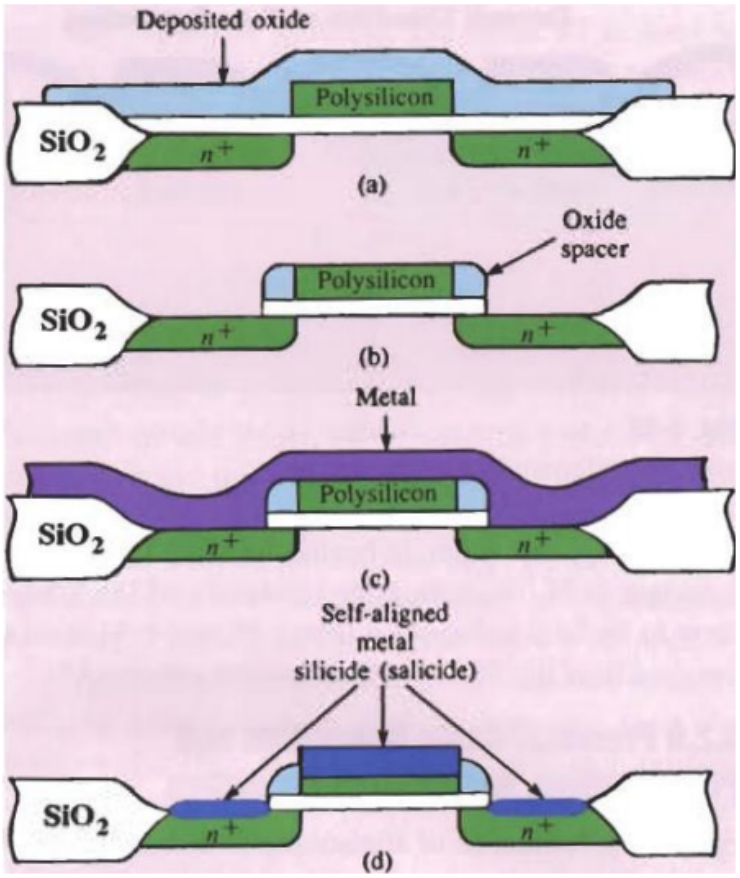


Figure 46:

102. Name two reasons that make silicon nitride suitable as a top passivation (or overcoat) layer for integrated circuit devices.

1. Chemically inert
2. Very Hard

103. What is chemical mechanical polishing, and what is it used for?

To polish? See the picture:

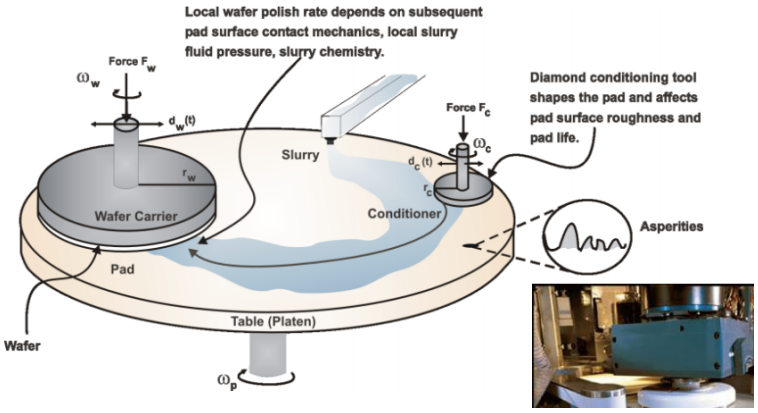


Figure 47:

Small particles (nm) of silica is the abrasive particles.

104. How can resistors, capacitors and inductors be realized with IC-technology?

"be realized?" I suppose it means manufactured/created/made...

Capacitor:
(a) Basically an highly doped semiconductor overgrown with oxide and coated with metal. Called **MOS- capacitor**
(b) A p-n junction with a large junction area. in reverse bias the space-charge region acts as diaelectric = "i motsatt riktning fungerar rymdladdningsregionen som dielektrisk". This one is called **p-n junction capacitor**
Inductors:
Not much info on the PP. Inductors resist change in the flow of current and are important in analog circuits and signal processing. They are flat.
Resistors:
See PP!!! Lecture 6

105. Describe the basic functionality of a flash memory cell.

Basically a transistor that traps a charge in the gate.

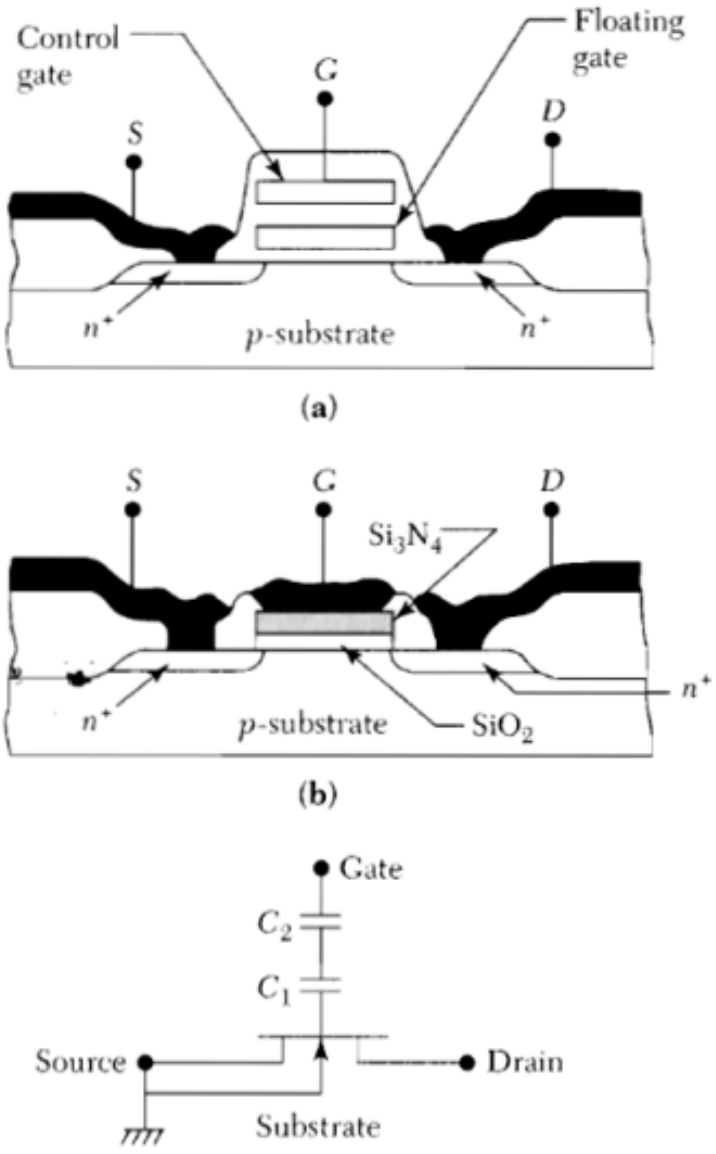


Figure 48:

Functionality? Described very well here:

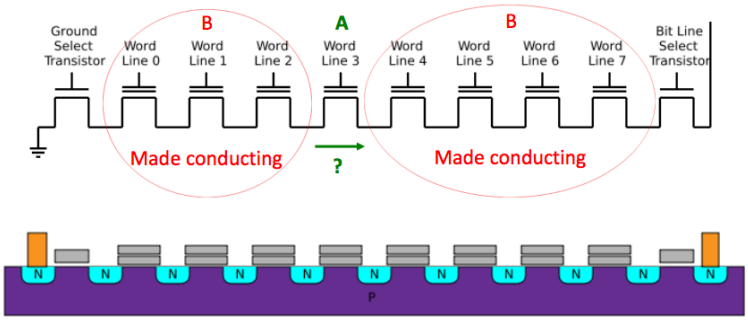


Figure 49:

106. Make a side-view sketch that describes the basic steps to how a suspended (freehanging, supported at the ends) structure can be realized that could be used in MEMS.

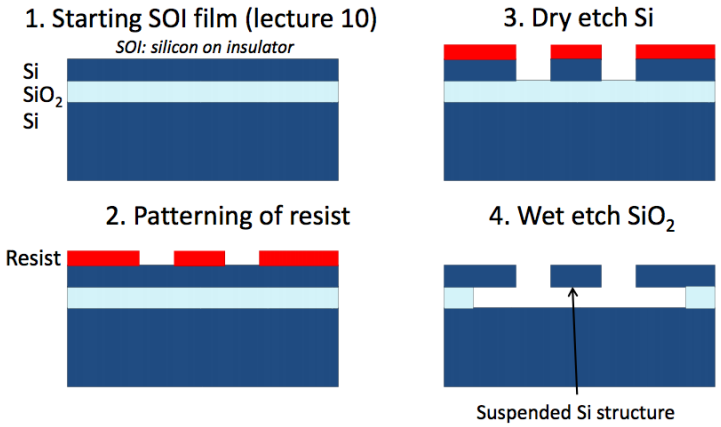


Figure 50:

107. Give a few examples of application areas of MEMS.

Projectors, Gyroscope, Micromotors.

Lecture 12

108. What is the purpose of wire-bonding?
Are there any alternatives to wire-bonding?

The purpose is to connect the chip ti the rest of the computational structure. The alternative is chip stacking

Advantages:
- Less space
- Shorter connections
- More integration in one package (MEMS, memory, etc)

Disadvantages:
- Risk of overheating
- Complexity: More complexwirebonding/soldering, dies need to be thinned

109. What determines the color of an LED?
How do we get a white LED?
(note: more than one possibility).

The bandgap determines the colour of the LED. How do we create white?
1. Mix green, blue and red LED
2. Use the blue (InGaN) one, then use phosphor to absorb blue light and emits a wide range of yellow and thereby creates white

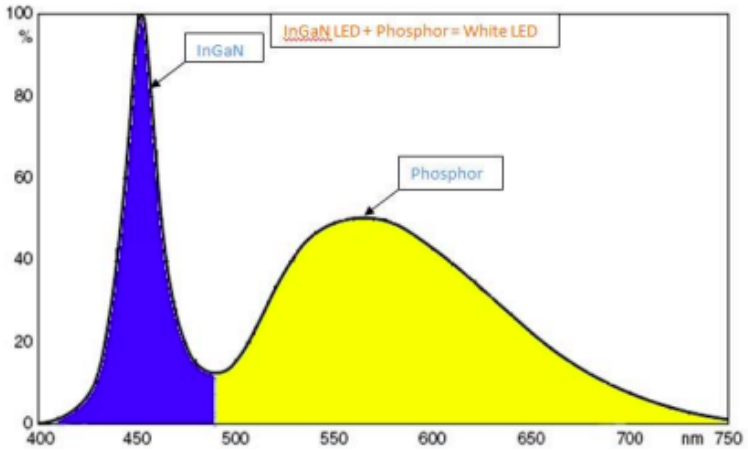


Figure 51:

110. How can an LED structure be modified to
obtain a laser?

You create a thin quatum-well that creates a small wide range of wavelength. You also need an optical captivity $\approx 300\mu m$. This is created by an optical active region (quantum-well) contained by 2 optical inactive regions. The structure also has one opening to let the light out. Some poits from PP:
- High p- and n-doping for population inversion
- The change in refractive index provides wave-guiding
- Reflection planes provides stimulated emission

111. Which is the most common solar cell material, why?

Si, cheap.

112. How can a solar cell be engineered to
extract more power from the sun?

Different materials at different depths, to extract energy from the different wavelengths.

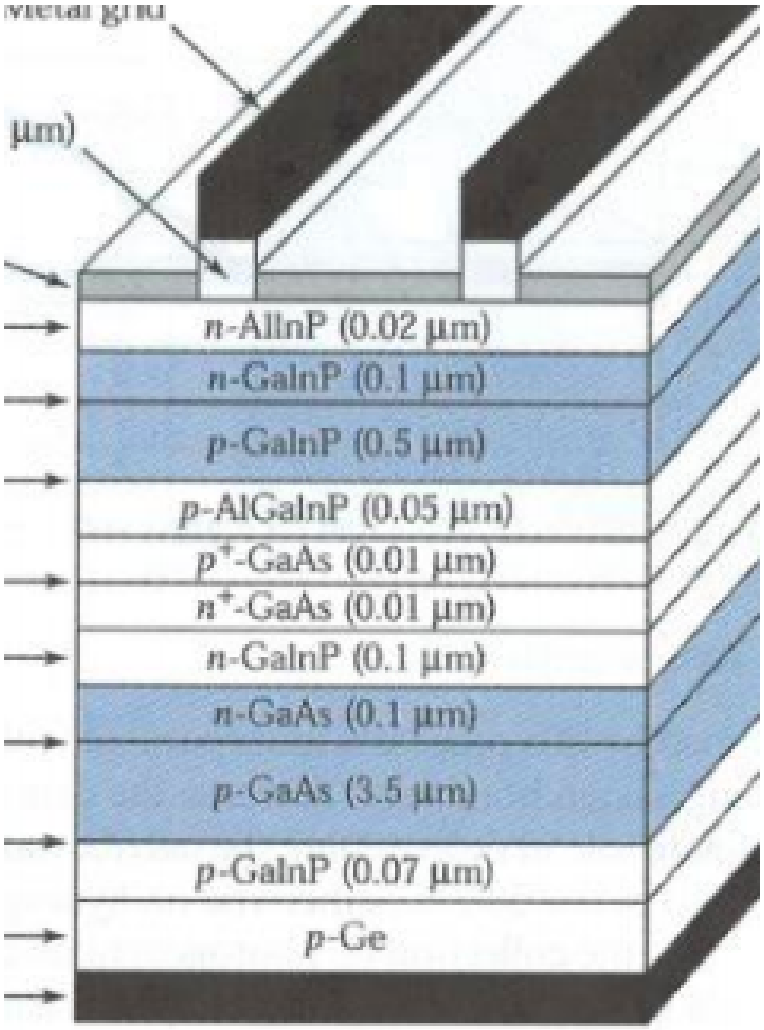


Figure 52:

113. Briefly outline the main steps in the fabrication of a crystalline Si solar cell.

1. Receiving of wafers and inspection
2. Chemical etching and texturization
3. Emitter diffusion
4. p-glass removal
5. Silicon nitride arc
6. Frontside printing
7. Backside printing
8. Classification and sorting